1. Product Overview

This specification defines the detailed requirements for the hybrid integrated circuits **DD1A401-24N12-S-531(F)** type radiation-hardened DC/DC converters (here in after referred to as circuits).
This specification specifies the requirements for circuits of two quality levels: H and QJB(G).

Note: Product images may not highlight current product markings

2. Referenced Documents

The following documents, in whole or in part, are referenced in this specification and are indispensable for its application. For dated or edition-referenced documents, subsequent amendments (excluding errata) or revisions do not apply. However, parties using this specification are encouraged to explore the possibility of using the most recent edition. For undated or edition-referenced documents, the latest edition of the referenced document applies.

GJB 548C-2021 Test Methods and Procedures for Microelectronic Devices
GJB 2438B-2017 General Specifications for Hybrid Integrated Circuits
SJ 20646-1997 Test Methods for DC/DC Converters of Hybrid Integrated Circuits
QJ 10004A-2018 Total Dose Irradiation Test Methods for Aerospace Semiconductor Devices
QJ 10005A-2018 Guidelines for Heavy Ion Single-Event Effect Tests on Aerospace Semiconductor Devices

3. Requirements

3.1 General Provisions

The circuit shall comply with all requirements specified in this specification and GJB 2438B-2017. In case of any discrepancy between the requirements of this specification and general specifications, this specification shall prevail.

3.2 Design, Structure, and Dimensions

3.2.1 Manufacturing Process

The circuit adopts a thick-film hybrid integration process, bare chip assembly, and a fully sealed metal casing.

a) The substrate material of the circuit is Al2O3, and the film resistors are printed using thick-film resistor paste.
b) The substrate and casing are reflow soldered. Power MOSFETs, Schottky diodes, and some surface-mount capacitors are reflow soldered to the substrate; some surface-mount capacitors are bonded to the substrate using conductive adhesive; power semiconductor chips such as power MOSFETs and Schottky diodes are bonded using Al wire; non-power semiconductor chips such as diodes, transistors, and PWM controllers are bonded to the substrate using conductive adhesive and Au wire; the transformer and the casing base are bonded using insulating adhesive.
c) The outer shell is sealed using a parallel seam welding process.

3.2.2 Absolute Maximum Ratings

Table 1. Rated conditions

Parameter	Symbol	Min	Max	Unit	Notes
Output power	P_O	-	44	W	
Input voltage	V_I	-	60	V	
Storage temperature	T_{stg}	-65	+150	V	
Lead Welding temperature	T_h	-	300	℃	10s

Note: Two or more absolute maximum ratings cannot be applied to the device simultaneously.

3.2.3 Recommended Operating Conditions

Table 2. Recommended operating conditions

Parameter	Symbol	Min	Max	Unit	Notes
Input voltage	V_I	20	50	V	
Output current	I_O	0.3	3.3	A	
Storage temperature	T_c	-55	+150	V	

3.2.4 Housing Appearance

The circuit adopts a metal dual in-line package. The housing appearance and dimensions of DD1A401-24N12-S-531 shall conform to the specifications in Figure 1.
The housing appearance and dimensions of DD1A401-24N12-S-531F shall conform to the specifications in Figure 2.

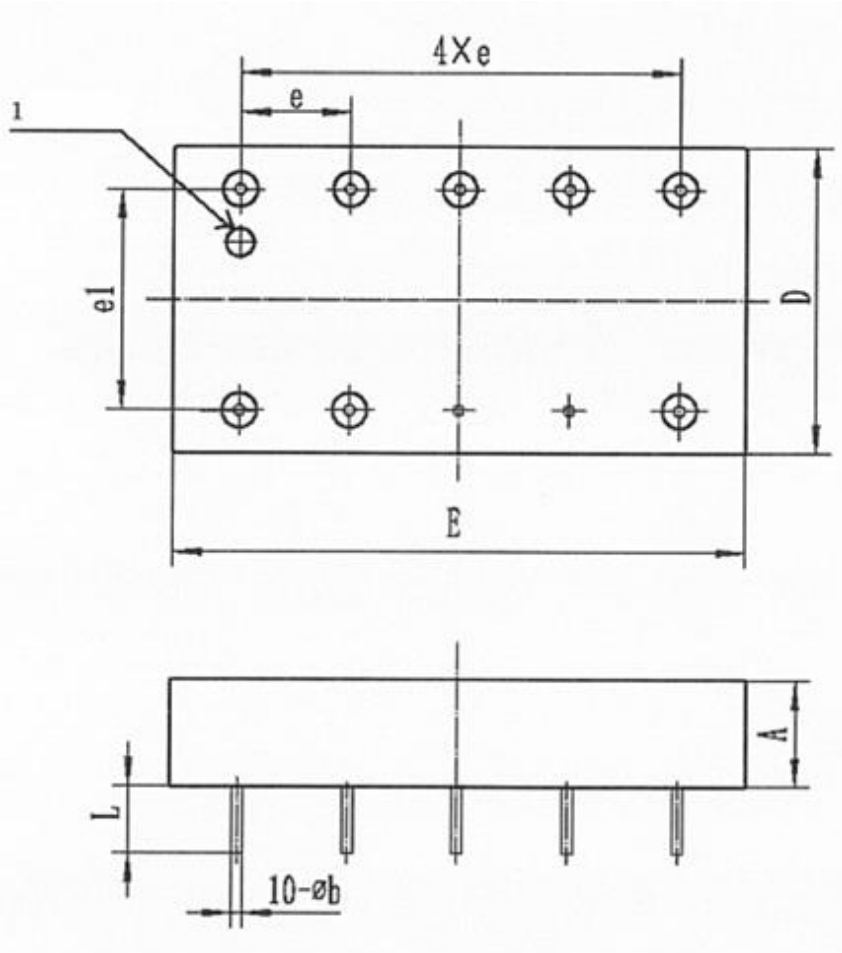


Figure 1. Dimensions of DD1A401-24N12-S-531

Table 3. Dimensions of DD1A401-24N12-S-531

Symbol	Value		
	Minimum	Nominal	Maximum
A		9.86	10.16
ϕb	0.87	1.00	1.13
D		28.19	28.69
E		53.08	53.58
e		10.16	
e1		20.32	
L	5.35	6.35	

Note 1: e and e1 are interchangeable dimensions, guaranteed by the manufacturing and inspection of the casing, and are not subject to testing requirements in this specification.

Note 2: During testing, only the minimum and maximum limit values are used as the criteria for acceptance; nominal values are not subject to testing requirements.

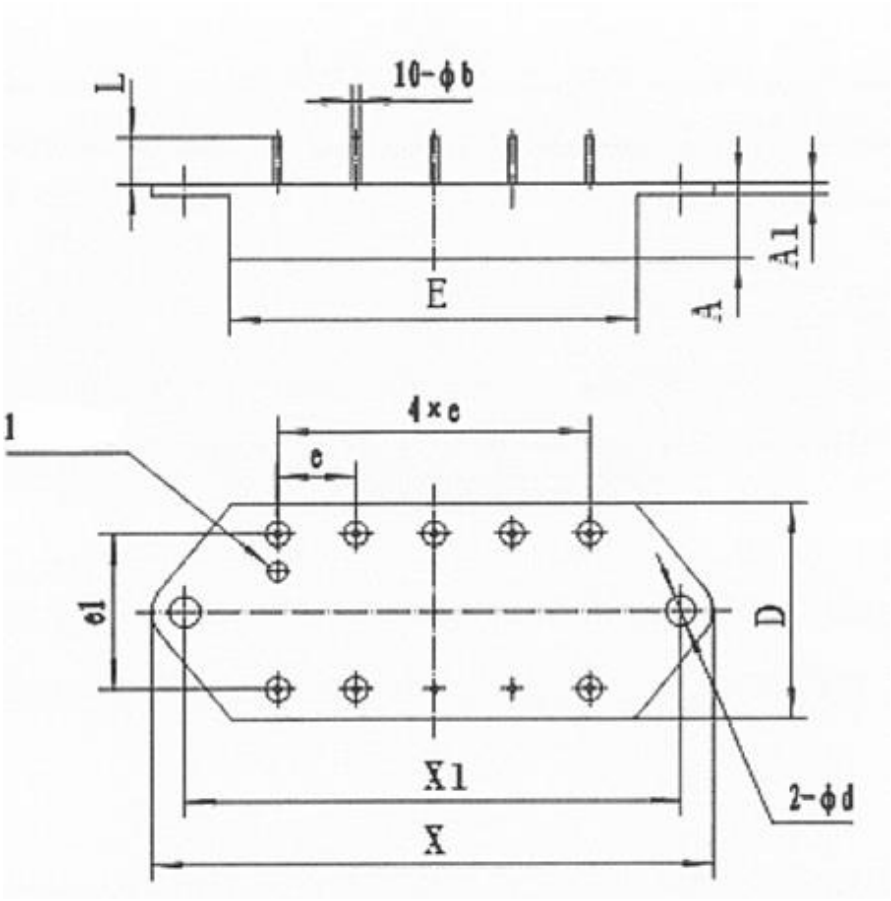


Figure 2. Dimensions of DD1A401-24N12-S-531F

Table 4. Dimensions of DD1A401-24N12-S-531F

Symbol	Value		
	Minimum	Nominal	Maximum
A		9.96	10.16
A1	1.30	1.50	1.70
ϕb	0.87	1.00	1.13
ϕd	3.90	4.10	4.30
D		28.19	28.69
e		53.08	53.58
E		10.16	
e1		20.32	
L	5.35	6.35	
X		73.41	73.91
X1	64.57	64.77	64.97

Note 1: e and e1 are interchangeable dimensions, guaranteed by the manufacturing and inspection of the casing, and are not subject to testing requirements in this specification.
Note 2: During testing, only the minimum and maximum limit values are used as the criteria for acceptance; nominal values are not subject to testing requirements.

3.2.5 Lead-out terminal arrangement

The lead-out terminal arrangement shall be as specified in Figure 3.

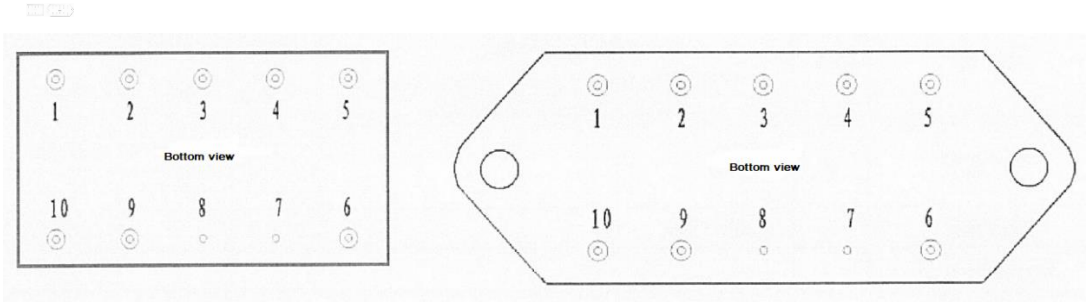


Figure 3. Lead-out arrangement

Table 5. Pin designations

Pin NO.	Label	Function	Pin NO.	Label	Function
1	V_I	Input Positive Terminal	7	SENSE+	Positive sensing terminal
2	INH	Inhibit Terminal	8	CASE	Casing ground
3	Sense-	Negative Sensing Terminal	9	CASE	Casing ground
4	GND_O	Output Ground Terminal	10	SYNC	Synchronization terminal
5	V_O	Output Positive Terminal	11	GND_O	Input ground terminal

3.2.6 Housing Material and Plating

The housing substrate is made of cold-rolled steel with a silver plating. The lead substrate is 4J50 copper-clad steel. The lead-out terminals are plated according to the specifications in GJB2438B-2017, 3.4.6.2.6, with gold plating on the lead surface. The gold plating thickness is 1.3 μm to 5.7 μm (leads 7 and 8 are the housing terminals and are wedge-plated). The functional block diagram should conform to the specifications in Figure 4.

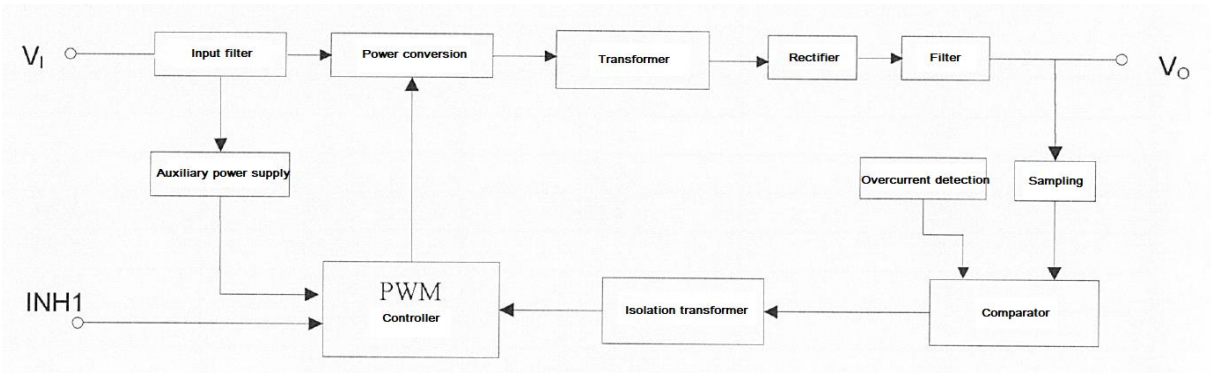


Figure 4. Functional block diagram

3.3 Weight

DD1A401-24N12-S-531 device weight: 49g±5g;
DD1A401-24N12-S-531F device weight: 52g±5g.

3.4 Electrical Specifications (Unless otherwise specified, −55℃ ≤T_C≤125℃, V_I=28V±0.5V and V_I=42V±0.5V, Inhibit load open, C_L=0)

The electrical characteristics shall conform to the specifications in Table 6.

Table 6. Electrical parameters

Parameters	Symbol	Min.	Max.	Unit	Group	Notes
Output voltage	V_O	11.88	12.12	V	1	I_O=3.3A
		11.64	12.36		2,3	
Output current	I_O	-	3300	A	1,2,3	V_I=20V...50V
Output ripple(peak-peak)	V_R	-	100	mV	1	BW=10kHz...6MHz, I_O=3.3A
		-	150		2,3	
Line regulation	S_V	-	50	mV	1,2,3	V_I=20V→50V, I_O=3.3A
Load regulation	S_I	-	50	mV	1,2,3	I_O=0→3.3A
Input current	I_{IN}	-	12	mA	1,2,3	Full load, prohibit connection from the input terminal.
		-	75			No load, no open circuit allowed
Input reflected ripple current(peak-peak)	I_{RIP}	-	80	mA	1	BW=20MHz, I_O=3.3A, connected to EMI filter
		-	100		2,3	
Input reflected ripple voltage(peak-peak)	V_{RIP}	-	500	mV	1,2,3	BW=20MHz, I_O=3.3A, connected to EMI filter
		-				
Switching frequency [b]	f_s	350	500	kHz	4,5,6	V_I=28V, I_O=3.3A
Efficiency	η	80	-	%	1,2,3	Input voltage V_I=28±0.5V: I_O=3.3A
		80	-			Input voltage V_I=42±0.5V: I_O=3.3A
Power dissipation	P_D	-	14	W	1,2,3	V_I=28V, Output short circuit
		-	16		1,2,3	V_I=42V, Output short circuit
Capacitance load[ab]	C_L	-	1000	μF	4	T_A=25°C, V_I=28V±0.5V, No effect on DC perf.
Isolation[g]	R_{ISO}	100	-	Mohm	1	T_A=25°C, Apply a 500V DC voltage between the input and output terminals and between any of the leads and the casing (except for terminals 7 and 8).
Vout response to load step[bc] (peak)	V_{LOR}	-600	600	mV	4	T_A=25°C, 50%load→ full load or full load→50%l. 10%load→50%load or 50%load→10%l.
Recovery time of Vout response to load step[bcd]	t_{LOR}	-	800	μs	4	T_A=25°C, 50%load→full load or full load→50%l. 10%load→50%load or 50% load→10%l.
Vout response to Vin step(peak)[be]	V_{VOR}	-600	600	mV	4	T_A=25°C, Input voltage V_I : 20V→50V,I_O=3.3A Input voltage V_I : 50V→20V, I_O=3.3A

Parameters	Symbol	Min.	Max.	Unit	Group	Notes
Recovery time of Vout response to Vin step[bde]	T_{VOR}	-	600	μs	4	T_A=25°C, Input voltage V_I : 20V→50V,I_O=3.3A Input voltage V_I : 50V→20V, I_O=3.3A
Start-up overshoot[b] (peak)	V_{TO}	-	120	mV	4,5,6	Input voltage V_I: 0→28V,I_O=3.3A
		-	120	mV	4,5,6	Input voltage V_I: 0→42V,I_O=3.3A
Start-up delay[f]	t_{TR}	-	10	ms	4,5,6	Input voltage V_I: 0→28V,I_O=3.3A
		-	10	ms	4,5,6	Input voltage V_I: 0→42V,I_O=3.3A
Load failure recovery time[bd]	t_{LF}	-	10	ms	4	T_A=25°C, I_O From short circuit to 3.3A
Inhibit input	V_{INH}	-	16	V	1	T_A=25°C, I_O=3. 3A, Prohibition of opening the end circuit
Protection power	P_W	44	-	W	1	T_A=25°C, I_O≥3.3A
External synchronization frequency range[b]	f_{SYNC}	400	500	kHz	4	T_A=25°C, I_O=3.3A, Pin 9 connect TTL level (5.5V≥V_{IH}≥4.5V, 0V≤V_{IL}≤0.8V) Duty cycle 40%...60%

Notes:

[a] Capacitive load does not affect DC parameters;

[b] This parameter is guaranteed by design and is only tested during identification inspection and design or process changes;

[c] The load jump time should be greater than 10ns;

[d] The recovery time refers to the time from the start of the jump until the output voltage returns to the corresponding stable value within the range of ±1%;

[e] The input voltage jump time should be greater than 200 μs;

[f] The start-up delay time can be calculated from the start of the power jump or from the disconnection of the grounded prohibition terminal;

[g] The test time is 1s. If the instrument displays qualified data, it is qualified. If the displayed data is unqualified, extend the test time to 60s. If the instrument displays qualified data, it is qualified.

Table 7. Table of electrical properties (Unless otherwise specified, T_A=25℃)

Parameters	Symbol	Min.	Max.	Unit	Group	Notes
Induction end impedance[a]	R_{Sense}	95	105	Ohm	7	Without power, the impedance between pin 3 (probe positive) and pin 4 (probe negative) is as follows
						Without power, the impedance between pin 6 (probe positive) and pin 5 (probe negative) is as follows

a) This parameter is guaranteed by the design; the impedance test at the inductor is performed after electrical tests at each stage.

For electrical parameters that require a range of variation, the permissible range of variation is shown in Table 8.

Table 8. Permissible range of electrical parameters

Parameter	Symbol	Condition (Unless otherwise specified, T_A=25°C, V_I = 28V ± 0.5V, no open circuits allowed, C_L = 0)	Allowable change rate of electrical parameters	Unit
Output voltage	ΔV_O	Fully loaded	±1	%
Efficiency	Δn	Fully loaded	±2	%

3.5 Electrical Testing Requirements

The electrical testing requirements for the circuit shall be as specified in Table 9, and the tests for each group shall be conducted in accordance with the provisions of Table 6 of this specification.

Table 9. Electrical Test Requirements

Test requirements	Grouping
Electrical test (before aging)	A1, A4
Final electrical test (after burn-in)	A1[a], A2, A3, A4, A5, A6, A7
Group A electrical test requirements	A1, A2, A3, A4, A5, A6, A7
Group C endpoint electrical test	A1, Δ limit[b] (for steady-state lifetime only)
Group E endpoint electrical test	A1

Notes:

[a] This packet computes the PDA.

B Steady-state life test A l group requires testing of the change in magnitude (Δ), and the limit of the change is specified in Table 8.

3.6 Electrostatic Discharge Sensitivity

The electrostatic discharge voltage is 2000V. ESD testing is only performed during qualification testing and when there are changes in design or process.

3.7 Circuit Marking

Circuit marking shall comply with the provisions of 3.4.6 in GJB2438B-2017. The marking content shall include the circuit type, first lead identification, batch number, electrostatic discharge identification, circuit serial number, quality grade, etc.

3.8 Irradiation Performance

The steady-state total dose shall not be less than 100 krad (Si), and the single-particle (burnout) dose shall not be less than 75 MeV • cm^2/mg.

4 Quality Assurance Provisions

4.1 Sampling and Inspection

The sampling and inspection procedures shall comply with the provisions of GJB2438B-2017 and this specification.

4.2 Screening

Before qualification and quality consistency testing, all circuits shall be screened according to C.4 of GJB2438B-2017 and Table 10 of this specification. Unless otherwise specified, the methods used in the table refer to the test methods in GJB 548C-2021.

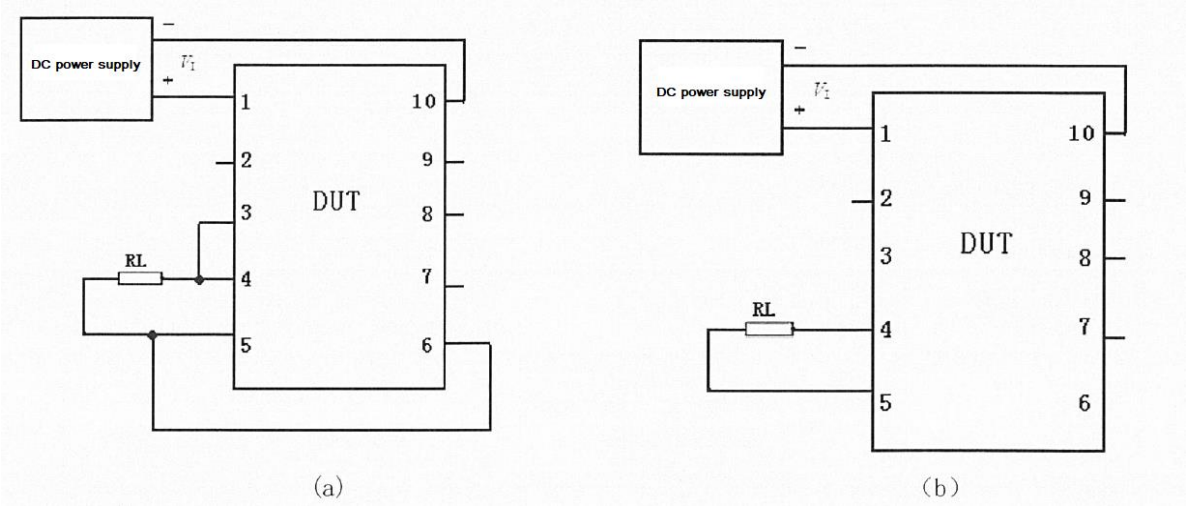
Table 10. Screening

Group	Test	GJB548C-2021		
		Method	Condition	
			H-class	QJB(G)
1	Internal visual inspection (before capping)	2017	Condition K	Condition K
2	Stability baking (before capping)	1008	150℃, at least 24h or 125℃, at least 168h	150℃, at least 24h or 125℃, at least 168h
3	Temperature cycling	1010	Condition C, -65℃ … 150℃, number of cycles: 10	Not Applicable
4	Constant Acceleration	2001	29400m/s², Y1 direction	Not Applicable
5	Particle collision noise detection (PIND)	2020	Condition A (after 40Hz)	Not Applicable
6	Electrical testing before aging [a]	-	As specified in Table 9 of this specification	As specified in Table 9 of this specification
7	Aging	1015	T_c=125℃, 160h, full load. Aging test circuit diagram is shown in Figure .	T_c=125℃, 48h, full load. Aging test circuit diagram is shown in Figure .
8	Electrical testing after aging	-	As specified in Table 9 of this specification	As specified in Table 9 of this specification
9	Permissible non-conforming rate (PDA) [b]	-	5% or 1 (whichever is greater)	5% or 1 (whichever is greater)
10	Sealing (fine leak detection and coarse leak detection)	1014	Fine leak test: A1 Pressure: 310kPa±15kPa, Pressure time: 4h, $R_1 \leq 3*10^{-3}$ Pa*cm³/s (He) Coarse leak test: Cl	Fine leak test: A1 Pressure: 310kPa±15kPa, Pressure time: 4h, R1 ≤ 3*10-3 Pa*cm³/s (He)

Group	Test	GJB548C-2021		
		Method	Condition	
			H-class	QJB Level 6
11	X-ray imaging	2012	X and Y directions	Not applicable
12	External visual inspection	2009	-	-

a) Pre-aging electrical testing can eliminate devices with non-compliant electrical parameters, but the number of eliminated items is not included in the non-conforming rate.

b) Typical failure refers to the failure of multiple devices within an aging batch that share the same fundamental cause. PDA and typical failure data only consider static test data (A1 group) of devices at 25°C.



Note 1: Select line connection method (a) or (b);
Note 2: V_I=28V±1V, A=3.6*(1±10%) Ohm (≥60W) or load current=3.3 X (1±10%) A.

4.3 Verification and Inspection

Verification and inspection shall be conducted in accordance with the provisions of this standard, and the inspections performed shall meet the requirements of groups A, B, C, D, and E of this standard.

4.4 Quality Consistency Inspection

The quality consistency inspection of Class H circuits shall be conducted in accordance with the provisions of this specification, and the inspection shall meet the requirements of Groups A, B, C, D, and E of this specification.

Quality consistency inspection of Class QJB (G) circuits is not required.

4.4.1 Group A Inspection

Group A inspection shall meet the requirements of Table 11.

Table 11. Group A inspection

Group	Test item	n (0)
A1	Static Test at 25°C	116 (0)
A2	Static Test at Maximum Rated Operating Temperature	76 (0)
A3	Static Test at Minimum Rated Operating Temperature	45 (0)
A4	Dynamic Test at 25°C	116 (0)
A5	Dynamic Test at Maximum Rated Operating Temperature	76 (0)
A6	Dynamic Test at Minimum Rated Operating Temperature	45 (0)
A7	Functional test at 25°C	116 (0)

Notes: The samples tested in Group A should be those that have passed screening. When the required sample size exceeds the batch size, 100% testing is permitted. After testing of Group A1 is completed, testing of the remaining Group A subgroups may be performed in any order.

4.4.2 Group B Test

Group B testing shall meet the requirements of Table 12. Each group test may use the screened electrical performance non-conforming products from the same inspection batch as samples.

Table 12. Group B test

Group	Test	GJB 548B-2005		Number of samples (Received samples)	GJB2438B-2017 chapter
		Method	Condition		
1	Dimensions	2016	Comply with 3.2.4 of this specification	2(0)	-
2	Solvent resistance [a]	2015	-	3(0)	-
3	Internal visual inspection and mechanical inspection	2014	-	1(0)	C.5.3.3.2
4	Bonding strength a) Hot pressing welding b) Ultrasonic welding	2011	Condition D	2 (0), Key thread count is 22 (0), If less than 22 (0), count as all	C.5.3.3.3
5	Chip shear strength	2019	-	2 (0), According to the number of components, it is 22 (0).If it is less than 22, it is all	C.5.3.3.4
6	Weldability[b]	2003	Solder temperature, 245°C±5°C	1 (0), 15 leads, if insufficient, all leads	C.5.3.3.5
7	Sealing [c] a) Fine leak detection b) Coarse leak detection	1014	Table 10, level H	15 (0)	C.5.3.3.6

a) Laser printed marking is not applicable;
b) Silver-plated leads, tin-plated pretreatment;
c) This test may be omitted if it is carried out between the final electrical test and the external visual inspection of the screening.

4.4.3 Group C Test

Group C tests shall be conducted in accordance with C.5.3.4 of GJB 2438B-2017 and Table 13 of this specification. Unless otherwise specified, the methods used in the table refer to the test methods of GJB 548C-2021.

Table 13. Group C test

Group	Test	GJB 548B-2005			Number of samples (Received samples)	GJB2438B-2017 chapter
		Method	Condition			
			QCI	Identification and testing		
1	Resistance to welding heat [a]	2036	Condition A		5(0)	C.5.2.4.6
	External visual inspection	2009	-			-
	PIND	2020	Not applicable	Condition A (40Hz for households), 5 passes		C.6.4.5.2
	Temperature cycle	1010	Condition C			C.6.4.5.3
			10 loops	100 loops		
	Constant acceleration or mechanical shock	2001 or 2002	Y1 direction, 1500g, 0.5ms, 5 times			C.6.4.5.5
			or 29400m/s², Y1 direction	**and** 49000m/s², Y1 direction		
	Random vibration	2026	Not applicable	Condition F: No power is applied during the test.		C.6.4.5.6
	Sealing a) Fine leak inspection b) Coarse leak inspection	1014	Same as Table 10, Level H			-
	PIND	2020	Not applicable	Condition A (40Hz for households), 1 pass		C.6.4.5.2
	Visual inspection	1010	1010, 4.3, 4.4			C.6.4.5.7
	Endpoint electrical test	-	According to Table 9 of this specification			C.6.4.5.8
2	Steady-state life	1005	T_c=125°C , 1000h, full load (Steady-state life test block diagram see Figure 5)		22 (0) or 5 (0) [b]	C.6.4.5.9
	End-point electrical test	-	According to Table 9 of this specification			C.6.4.5.8
3	Internal water vapor content [c]	1018	100°C, water vapor content is not more than 5000ppm		3 (0)	C.6.4.5.10
4	ESD [a] Electrical paramet. ESDS Electrical paramet.	3015	A1 grouping 2000V A1 grouping		3(0)	C.5.2.4.5

a) Only when the qualification test and subsequent design changes affect the test;
b) When it is a qualification test or a QCI for limited samples, the sample size (number of acceptances) can be 5 (0);
c) 3 samples were drawn from the group 1 samples after the experiment.

4.4.4 Group D test

Group D inspection shall be conducted in accordance with C. 5. 3. 5 of GJB 2438B-2017 and Table 14 of this specification. Unless otherwise specified, the methods used in the table refer to the test methods of GJB 548C-2021. Group D tests may use electrically non-conforming products or sealed empty casings screened from the same inspection batch. If the circuit casing passed the casing evaluation test upon arrival and the test items cover the tests specified in Table 14, then Group D inspection does not need to be repeated.

Table 14. Group D test

Group	Test	GJB 548B-2005		Number of samples (Received samples)	Illustrate
		Method	Condition		
D1	Thermal shock	1011	C	5(0)	
	Stability baking	1008	150°C, 1h		
	Lead firmness	2004	Condition B_1, Rigid lead		Only 1 (0) 15 leads, insufficient to represent the entirety.
	Sealing: a) Fine leak detection b) Coarse leak detect.	1014	Table 10, level H		
D2[a]	Salt spray	1009	Condition A	5(0)	
D3[a]	Metal shell insulation	1003	500V, max 80nA	3(0)	

a) Only performed during identification inspection or when housing material is changed.

4.4.5 Group E Test

Group E testing shall be conducted in accordance with the provisions of Table 15 of this specification.

Table 15. Group E inspection

Group	Test	Method	Test conditions	Sample size
E1 [ab]	Steady-state total dose Irradiation	QJ 10004A-2018	Not less than 100 krad (Si), dose rate 0.1 lk rad (Si) / s; irradiation test diagram and bias conditions are shown in Figure 6.	4 (0)
	Final electrical test		A1	

Group	Test	Method	Test conditions	Sample size
E2 [a]	Single-event effect (Burnout)	QJ 10005A-2018	The single-event failure threshold LET > 75 MeV cm²/mg. The single-event transient effect failure criterion is: the transient waveform amplitude is relatively stable; the waveform amplitude change is ±10% of the output voltage; and the minimum pulse width N is 5 ms. Both conditions must be met simultaneously. The irradiation test diagram and bias conditions are shown in Figure 6.	2 (0)

a) This procedure is only performed when identifying or when design or process changes that may affect the irradiation effect occur;
b) For Group E1, two devices are biased, and two devices are irradiated with all pins shorted without bias. One additional device of the same model and specifications is not irradiated for comparative testing.

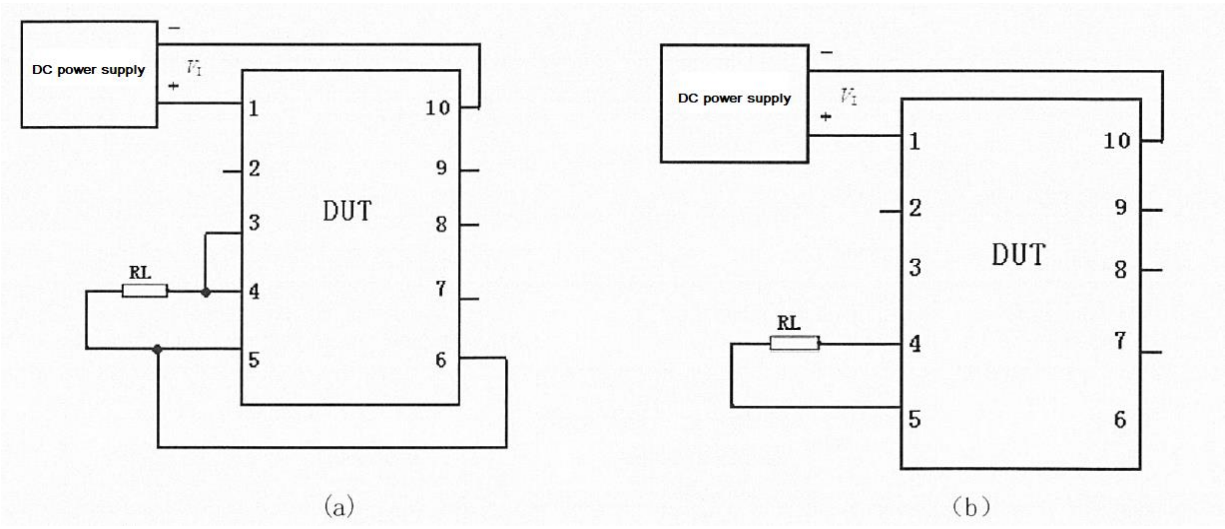


Figure 6. Irradiation test circuit diagram

Note 1: Circuit connection method selection (a) or (b);
Note 2: Total dose test bias conditions: V_I = 48V ... 50V, R_L = 18 Ohm ... 36 Ohm (choose one of the resistance values, power 210W) or use an electronic load instead;
Note 3: Single particle test bias conditions: V_I = 48V ... 50V, R_L = 3.6x(1±10%) Ohm (≥60W) or use an electronic load instead.

4.5 Destructive Physical Analysis (DPA)

DPA testing is conducted in a laboratory approved by both the supplier and the buyer, or upon the user's request, with two samples per sample. The DPA test items are as specified in Table 16.

Table 16. Destructive Physical Analysis (DPA)

Test		GJB 548C-2005	
		Method	Condition or requirement
External Visual Inspection		2009	-
X-Ray Inspection		2012	-
PIND		2020	Condition A (40Hz per household)
Seal	Fine leak	1014	Same as Table 10, Level H
	Gross leak		Condition C1
Moisture Content Test		1018	100°C, water vapor content not more than 5000 ppm
Internal Visual Inspection		2017	Condition K level
Scanning Electron Microscope (SEM) Inspection [a]		2018	-
Bond Strength		2011	-
Die Shear Strength		2019	-

Notes:

[a] If SEM has already been performed at the wafer level, it is not necessary to repeat.

4.6 Test Methods

4.6.1 Electrical Parameter Testing

Unless otherwise specified, the electrical parameters shall be tested in accordance with SJ 20646-1997 "Test Methods for Hybrid Integrated Circuit DC/DC Converters".

4.6.2 Test Block Diagram

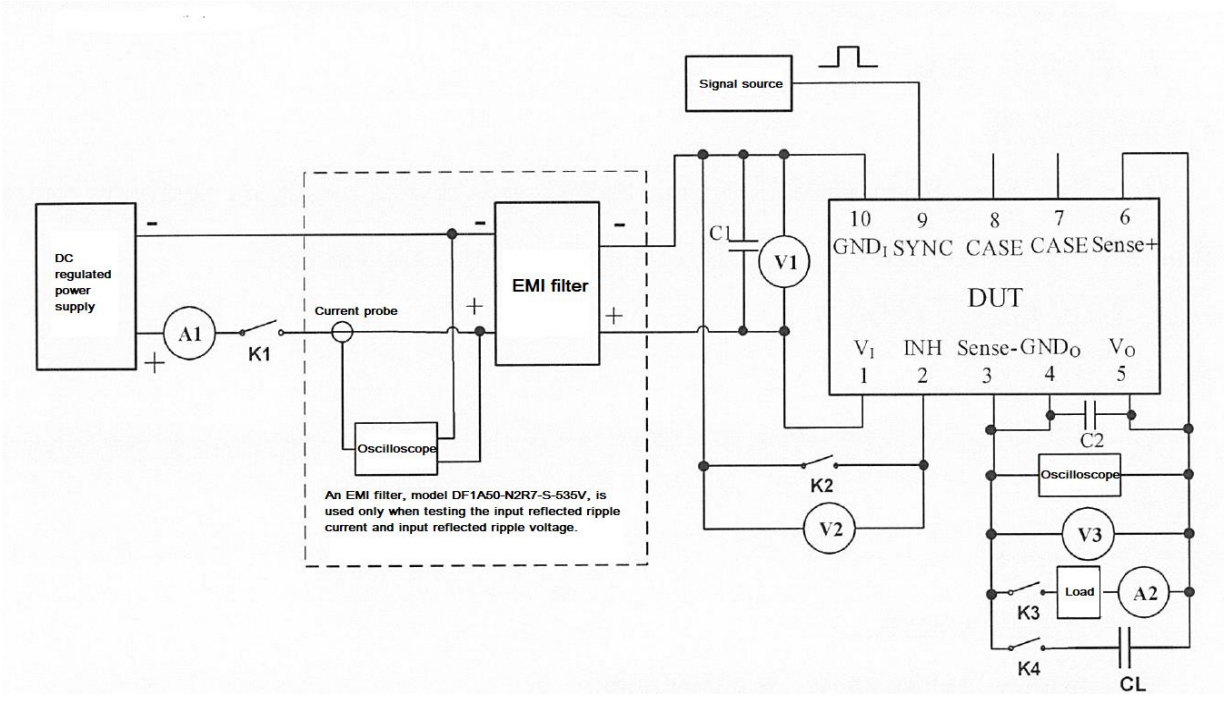


Figure 7. Test circuit block diagram

Note 1: C_1 = 0 ... 10 uF; C_2 = 0 ... 10 pF;
Note 2: Description of the prohibited terminal status during testing: The prohibited terminal switch K2 is only closed according to the test conditions when testing the input current index; otherwise, the prohibited terminal switch is open.

4.6.3 Main Testing Instruments

a) Power Supply: Output voltage ≥80V, output current ≥3A;
b) Electronic load: output current ≥ 10A.
c) Oscilloscope: bandwidth ≥ 100MHz;
d) Voltmeter, ammeter: digital multi-purpose meter with accuracy of 4.5 digits or above;
e) High resistance meter: Output voltage > 500V.

4.6.4 Room temperature and high/low temperature tests of the product

a) Room temperature test: The product should be placed in an environment of 25℃ to reach a stable state before testing its electrical performance;
b) High temperature test: The product should be placed in a high-temperature chamber at 125℃ for 30 minutes, then removed and its electrical performance measured;
c) Low temperature test: The product should be placed in a low-temperature chamber at -55℃ for 30 minutes, then removed and its electrical performance measured.

4.6.5 Input Reflected Ripple Current Test

4.6.5.1 Test Objective

Input reflected ripple current refers to the AC component of the input current flowing through the DC/DC converter, reflecting the impact of the DC/DC converter on the power supply.

4.6.5.2 Test Conditions

a) Ambient temperature: T_A = 25°C;
b) Power supply condition: V_I=28V±0.5V; V_I=42V±0.5V;
c) Load condition: full load.

4.6.5.3 Test Procedures

The test block diagram is shown in Figure 7. Connect the EMI filter, close switches KI and K3, set the oscilloscope to AC input, connect the current probe to the positive input terminal of the circuit under test, and read the peak-to-peak value of the measured current from the oscilloscope, which is the input reflected ripple current.

4.6.6 Input Reflected Ripple Voltage Test

4.6.6.1 Test Objective

Input reflected ripple voltage refers to the AC component of the input voltage of a DC/DC converter, reflecting the impact of the DC/DC converter on the power supply.

4.6.6.2 Test Conditions

a) Ambient temperature: T_A = 25°C;
b) Power supply condition: V_I=28V±0.5V; V_I=42V±0.5V;
c) Load condition: full load.

4.6.6.3 Test Procedure

The test block diagram is shown in Figure 7. Connect the EMI filter and close switches KI and K3. Set the oscilloscope to AC input and connect it to the input terminal of the circuit under test. Read the peak-to-peak value of the AC component of the input ripple voltage from the oscilloscope; this is the input reflected ripple voltage.

4.6.7 Short-Circuit Power Consumption Test

4.6.7.1 Test Purpose

To test the power consumption of the circuit when the output is short-circuited.

4.6.7.2 Test Conditions

a) Ambient temperature: T_A = 25°C;
b) Power supply condition: V_I=28V±0.5V; V_I=42V±0.5V;
c) Output terminal (short circuit at the root of the lead);

4.6.7.3 Test Procedure

The test block diagram is shown in Figure 7. Under the specified temperature conditions, connect the circuit to the test system. At this time, the circuit output voltage meets the requirements of Table 1. Set the input voltage to 28V or 42V. After short-circuiting the positive and negative output terminals, record the input voltage and input current values. The short-circuit power consumption is calculated as: $P_D=V_I x I_I$.

4.6.8 Capacitive Load Test

4.6.8.1 Test Purpose

To test the power consumption of the circuit when the output is short-circuited.

4.6.8.2 Test Conditions

a) Ambient temperature: T_A = 25°C;
b) Power supply condition: V_I=28V±0.5V; V_I=42V±0.5V;
c) Load condition: full load.
d) Capacitor capacitance: C_L≤1000uF;

4.6.8.3 Test Procedure

The test block diagram is shown in Figure 7. With switches KI, K3, and K4 closed, connect the circuit to the test system under the specified temperature conditions. Set the input voltage to 28V and the output current to the rated output current. Test the output voltage.. If the output voltage meets the requirements of Table 6, it is qualified.

4.6.9 Load Failure Recovery Time Test

4.6.9.1 Test Objective

Test the time it takes for the DC/DC converter output to recover to full load from a load failure.

4.6.9.2 Test conditions

a) Ambient temperature: T_A = 25°C;
b) Power supply condition: V_I=28V±0.5V; V_I=42V±0.5V;
c) Load condition: full load.

4.6.9.3 Test Procedure

The test block diagram is shown in Figure 6. With switches KI and K3 closed, connect the circuit to the test system under the specified temperature conditions. Input voltage/settings:
28V, 42V. Adjust the load from a short-circuit state to the rated output current state. Measure the instantaneous waveform of the re-established output voltage on the oscilloscope. The time it takes for the output voltage to recover to 90% of the rated output voltage after the fault is cleared is the load fault recovery time.

4.6.10 Open-Circuit Voltage Test of the Prohibition Terminal

4.6.10.1 Test Purpose

To test the prohibition terminal voltage when the prohibition terminal of the circuit is open.

4.6.10.2 Test Conditions

a) Ambient temperature: T_A = 25°C;
b) Power supply condition: V_I=28V±0.5V; V_I=42V±0.5V;
c) Load condition: full load.

4.6.10.3 Test Procedure

Under the specified temperature conditions, connect the device under test to the test system as shown in Figure 7, close KI and K3, and set the load to full load. Test the voltage and NH when the prohibition terminal is open.

4.6.11 Output Ripple Voltage Test

4.6.11.1 Test Purpose

To test the peak-to-peak value of the AC component contained in the DC output voltage.

4.6.11.2 Test Conditions

a) Ambient temperature: T_A = 25°C, T_C = -55°C, T_C = 125°C;
b) Power supply condition: V_I=28V±0.5V; V_I=42V±0.5V;
c) Load condition: full load.

4.6.1.1.3 Test Procedure

The test block diagram is shown in Figure 7. During the test, set the oscilloscope to AC test mode, with a bandwidth limited to 10kHz to 6MHz. Set the oscilloscope's test probe to the "XI" setting, and connect the positive output terminal and the output ground terminal of the power module to the product test board using the shortest grounding method (see Figure 8). Read the peak-to-peak voltage directly from the oscilloscope.

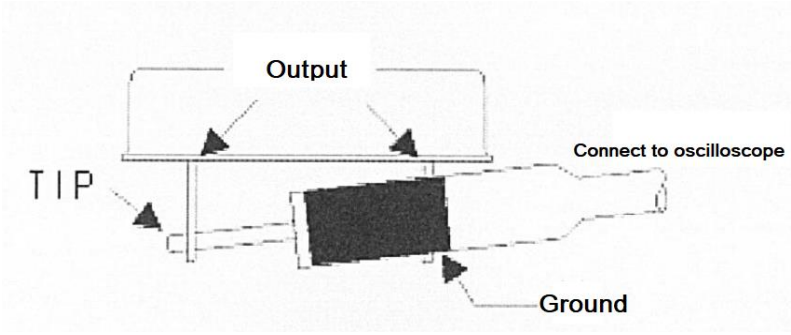


Figure 8. Recommended Testing Method

4.6.12 Protection Power Test

4.6.12.1 Test Objective

The test circuit output power has a load capacity of 1.1 times.

4.6.12.2 Test Conditions

a) Ambient temperature: T_A = 25°C;
b) Power supply condition: V_I=28V±0.5V; V_I=42V±0.5V;
c) Load condition: full load.

4.6.12.3 Test Procedure

Under specified temperature conditions, connect the device under test to the test system as shown in Figure 7; close K1 and K3, set the output current to be ≥ 1.1 times the rated output current, so that the output power reaches 1.1 times the rated output power, and test the output voltage 6. If the output voltage meets the requirements of Table 6, it is qualified.

4.6.13 Impedance Test of the Induction Terminal

4.6.13.1 Test Purpose

The impedance test of the induction terminal is performed after the electrical tests of each component. Its purpose is to confirm the reliability of the internal electrical connections of the induction terminal and ensure its normal function.

4.6.13.2 Test Conditions

a) Ambient temperature: T_A = 25°C;
b) Power supply condition: V_I=28V±0.5V; V_I=42V±0.5V;
c) Test instrument: Powered digital multimeter or impedance tester;

4.6.13.3 Test Procedure

T_A = 25℃. When the product is not in operation, use a digital multimeter or impedance tester to measure the impedance between the 3rd lead (probe positive) and the 4th lead (probe negative), and the impedance between the 6th lead (probe positive) and the 5th lead (probe negative). Note the direction of the positive and negative probes.

4.6.14 External Synchronization Frequency Range Test

4.6.14.1 Test Objective

Test products with synchronization input functionality. When an external synchronization input signal is input to the external synchronization input terminal, the operating frequency of the power supply module should be consistent with the frequency of the external synchronization input signal, and the output voltage should be normal.

4.6.14.2 Test Conditions

a) Ambient temperature: T_A = 25°C;
b) Power supply condition: V_I=28V±0.5V; V_I=42V±0.5V;
c) Load condition: full load.

4.6.14.3 Test Procedure

The test block diagram is shown in Figure 7. Under the specified temperature conditions, connect the circuit to the test system. Set the input voltage to 28V, the output current to full load, and connect a TTL signal of the specified frequency (0V≤V_{IL}≤0.8V, 4.5V≤V_{IH}≤5.5V) to the synchronization input, with a duty cycle of 40%...60%. Monitor the output voltage ripple frequency, which should be within the specified range.

5. Delivery Preparation

5.1 Packaging Requirements

Packaging requirements shall comply with the provisions of 5.1 in GJB 2438B-2017.

6. Notes

6.1 Intended Use

The hybrid integrated circuits conforming to this specification are intended for use in the design of new equipment and for technical support of existing equipment.

6.2 Contents to be Clarified in Ordering Documents

The contents of the contract and other ordering documents shall comply with the provisions of 6.2 in GJB 2438B-2017

6.3 Circuit Quality Assurance Level

The circuit quality assurance level is H and QJB(G) level, as specified in the 43rd Research Institute document QS/HW 30301 "Regulations on Quality Levels of Military Hybrid Integrated Circuit

6.4 Circuit Quality Control

The circuit design and structural design of the two quality level circuits specified in this specification should be completely identical. The products should be manufactured on a military standard production line of H level (or above) certified by GJB 2438.

7. Order guide

Table 17. Order Code

Company name	Type	Series name	Output Power	Input voltage	Outputs number	Output voltage	Temperature grade	Packaging options
D	D	1A	401	24	N	12	S	531
SmartPower	D: DC/DC	1A: Rad-Hard Module	201=20 251=25 301=30 401=40	24=20…50	Single	12 V	S = -55 … +125 °C	531 F=Flanged