SKYLIGHT

3300...4200MHz Low Power Pre-Driver Amplifier SI8B3312Q

The **SI8B3312Q** is a driver amplifier housed in a low-cost, 4×4mm LGA package. This product is specifically designed for 3.3 to 4.2GHz under a single 5V supply.
Optimized in-package impedance matching circuitry provides 50Ω nominal RF input and output impedance.
The device is used for LTE and NR base stations.

A block diagram of the **SI8B3312Q** is shown in Figure 1.
The device package and pinout are shown in Figure 2.
Signal pin assignments and functional pin descriptions are described in Table 1.

Applications:
5G m-MIMO, Mobile Infrastructure, General Purpose Wireless.

Main parameters:

1 Operating Frequency: 3300...4200GHz
2 P_{1dB}: 33dBm
3 Gain: 26.6dB
4 Dimension: 20-pin, 4×4×0.85mm LGA package
5 50Ω Matched RF Input and Output
6 Active bias control (adjustable externally)
7 Power down control via EN pin
8 5V supply

Table 1. SI8B3312Q Signal Description*

Pin	Name	Description	Pin	Name	Description
1,2, 4, 5, 10, 11, 12, 14, 15,16,17,19	NC	Not Used	9	VBIAS	Active bias collector
3	RF_{IN}**	RF input port	13	RF_{OUT}**	RF output port
6	EN	PA on/off logic control	18	VCC2	Stage 2 collector voltage
7	VB1	Stage 1 Bias control	20	VCC1	Stage 1 collector voltage
8	VB2	Stage 2 Bias control			

Notes:
*The center ground pad must have a low inductance and low thermal resistance connection to the application's printed circuit board ground plane;
**Neither of Pin3 and Pin13 has the blocking capacitor. They are DC grounded internal to the IC, because the first component in the package connected to the Pin3 and Pin13 is parallel inductor to GND. Do not apply voltage to the two pins.

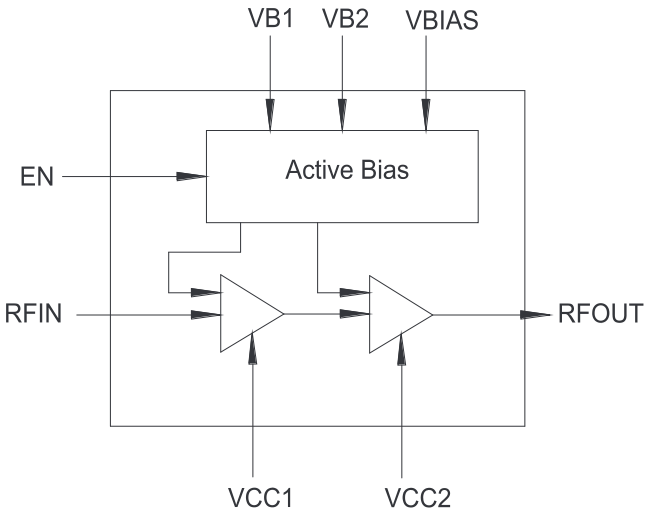

Fig. 1. SI8B3312Q Block Diagram

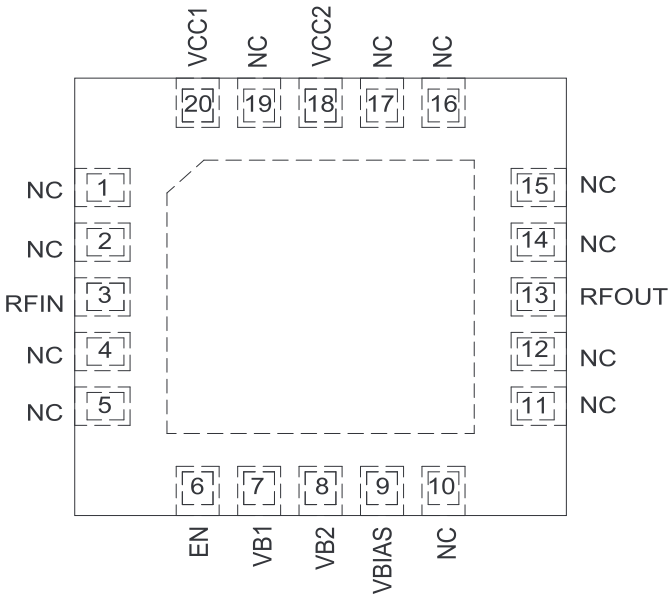

Fig. 2. SI8B3312Q Pinout (Top View)

Electrical and Mechanical Specifications

The absolute maximum ratings of the SI8B3312Q are provided in Table 2. Recommended operating conditions are specified in Table 3, and electrical specifications are provided in Table 4.

Table 2. SI8B3312Q Absolute maximum ratings (T_A=25°C)

Parameter	Symbol	Value			Remark
		Min.	Typ.	Max.	
RF input power (CW, 50Ω load)	P_{IN}	-	-	20	dBm
Supply voltage	V_{CC}	-	-	7	V
EN voltage	VEN	-	-	5	V
Operating temperature*	T_C	-40	-	115	°C
Storage temperature	T_{ST}	-65	-	150	°C
Junction temperature @MTTF=1E+06hr	T_J	-	-	165	°C

*When the ambient temperature is 115°C, PA works in on state, the max junction temperature on the GaAs die is about 132°C, the maximum SMD temperature in the package is about 124°C.

Table 3. SI8B3312Q Recommended Operating Conditions (T_A=25°C)

Parameter	Symbol	Value			Remark
		Min.	Typ.	Max.	
Supply voltage	V_{CC}	-	5	-	V
Operating frequency	f	3300	-	4200	MHz
Operating temperature	T_C	-40	25	115	°C

Table 4. SI8B3312Q Electrical Specifications*

Parameter	Symbol	Test conditions	Value			Unit
			Min	Typ	Max	
Frequency	f		3300	-	4200	MHz
Small signal gain @P_{in}=-30dBm	|S21|	3300...3800MHz	-	26.6	-	dB
		3800...4200MHz	-	26.6	-	dB
Gain flatness		3100...4400MHz (Any 100MHz)	-	0.3	-	dB
		3100...4400MHz (Any 400MHz)	-	0.7	-	dB
Gain @P_{out}=+21dBm		3300...3800MHz	-	26.8	-	dB
		3800...4200MHz	-	26.8	-	dB
Input return loss @P_{in}=-30dBm	|S11|	3300...4200MHz	-	15	-	dB
Output return loss @P_{in}=-30dBm	|S22|	3300...4200MHz	-	12	-	dB
Reverse isolation @P_{in}=-30dBm	|S12|	3300...4200MHz	-	45	-	dB

Table 4. SI8B3312Q Electrical Specifications (cont.)

Parameter	Symbol	Test conditions		Value			Unit
				Min	Typ	Max	
Output power at 1dB gain compression	P_{1dB}	3300...4200MHz 15% Duty Cycle(150μs/1ms), reference to small signal gain (P_{in}=-30dBm)		-	33	-	dBm
Saturated output power	P_{SAT}	3300...4200MHz 15% Duty Circle(150μs/1ms), Output power at 3dB gain compression		-	34	-	dBm
ACPR with DPD @+21dBm	Loop ACPR	2X100MHz, PAR=8.5dB	3500 MHz	-	-53	-	dBc
			3700 MHz	-	-54	-	dBc
			4200 MHz	-	-52	-	dBc
ACPR without DPD @+21dBm	ACPR	2X100MHz, PAR=8.5dB	3500 MHz	-	-32	-	dBc
			3700 MHz	-	-35	-	dBc
			4200 MHz	-	-32	-	dBc
Noise Figure*	NF	3300...4200MHz		-	5.7	-	dB
Gain full temperature variation		3300...4200MHz -40...115°C		-	3.5	-	dB
Vcc1 Quiescent current*	I_{CQ1}	No RF signal		-	65	-	mA
Vcc2 Quiescent current*	I_{CQ2}	No RF signal		-	190	-	mA
Thermal Resistance from Junction to Package Top	θ_{JT}	No RF signal, EVB is on the heat plate, tune heat plate temperature to make the EVB Board temperature is 120°C		-	6.5	-	°C/W
Thermal Resistance from Junction to Package Board*	θ_{JB}			-	13.5	-	°C/W
VB1 Quiescent current	I_{VB1}	No RF signal		-	2.5	-	mA
VB2 Quiescent current	I_{VB2}	No RF signal		-	2.8	-	mA
VBIAS Quiescent current	I_{VBIAS}	No RF signal		-	2.2	-	mA

Table 4. SI8B3312Q Electrical Specifications (cont.)

Parameter	Symbol	Test conditions	Value			Unit
			Min	Typ	Max	
Off VCC1 Leakage Current		VB1=VB2=0V, VCC1=VCC2=VBIAS=5V, VEN=1.8V	-	0.1	-	μA
Off VCC2 Leakage Current			-	0.1	-	μA
Off VBIAS Leakage Current			-	0.4	-	mA
EN Logic High	VEN	On State	1.17	-	5	V
EN Logic Low		Off State	0	-	0.63	V
Off VCC1 Leakage Current		VEN=0V, VCC1=VCC2=VBIAS= =VB1=VB2=5V	-	0.1	-	μA
Off VCC2 Leakage Current			-	0.1	-	μA
Off VBIAS Leakage Current			-	1.1	-	mA
Off VB1 Leakage Current			-	3.5	-	mA
Off VB2 Leakage Current			-	4	-	mA
Device ON or OFF Timing*		50% EN to 10/90% RF	-	600	-	nS
Impedance of EN Port		VEN=1.8V	1800	-	-	kΩ
Shutdown Voltage* (VB1+VB2+VBIAS)	VBoff	Reduce VB voltage until Quiescent current down to 0A	-	2.8	-	V

*Notes:

1. Test conditions unless otherwise noted: VCC1=VCC2=VB1=VB2=VBIAS=5V, VEN=1.8V, Temperature=25°C, 50Ω system.
2. Noise figure data hasn't input trace loss de-embedded.
3. I_{CQ1} and I_{CQ2} are adjustable externally through adjust resistors of VB1 and VB2 respectively, and the quiescent current is proportional to temperature.
4. The temperature of the EVB board near the package.
5. EN bypass capacitor C5 is 1nF.
6. When using LDMOS switch drive circuit to control VB (VB1+VB1+VBIAS) turning on and off the PA, the EVB capacitor C8 should be removed (decided by the LDMOS switch drive circuit), otherwise the switching speed will slow down. However, if C8 is removed, the Loop ACPR results will deteriorate.

Table 5. EN control management*

Logic level	Low	High
State	Off	On
Voltage	0...0.63V	1.17...5V

*When VEN is suspended, the device is in an on state.

Table 6. EN Voltage and Current (VCC1=VCC2=VB1=VB2=VBIAS=5V, Temperature=25°C)

VEN Voltage (V)	0	1.8	3.3	5
VEN Current (μA)	-103	0	0	0

Evaluation Board Description

An Evaluation Board schematic is provided in Figure 3. Table 7 provides the Bill of Materials (BOM) list for Evaluation Board components.

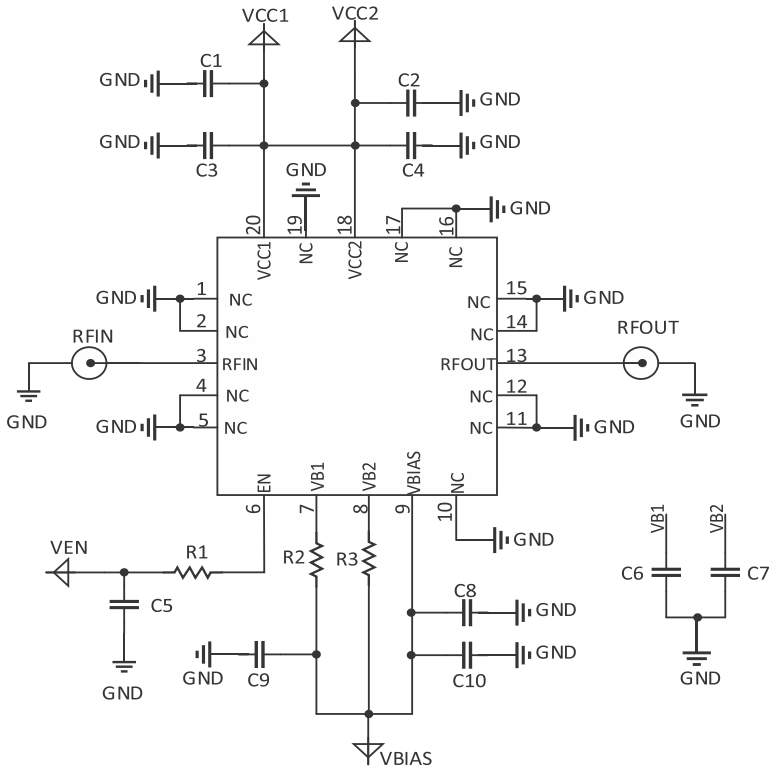

Fig. 3. SI8B3312Q Application Schematics

Note: The application schematics is for reference only, and the customer can modify it according to the actual situation.

Table 7. SI8B3312Q Evaluation Board Bill of materials

Component	Description	Size
C4, C8	Ceramic capacitor, 1μF, 16V, ±20%, X7S	0402
C5	Ceramic capacitor, 1nF, 50V,±5%, COG	0402
R1	Resistor, 0Ω, 0.0625W	0402
R2, R3	Resistor, 150Ω, 0.0625W	0402
C1, C2, C3, C6, C7, C9, C10	NC	

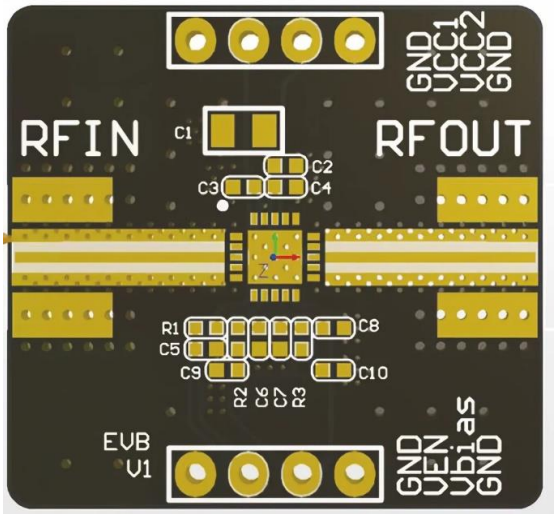

Fig. 4. Evaluation Board Assembly Drawing

Typical Performance Plots

Test conditions unless otherwise noted: VCC1=VCC2=VB1=VB2=VBIAS=5V, VEN=1.8V, Temperature=25°C, Frequency: 3300-4200MHz, Rload=50Ω

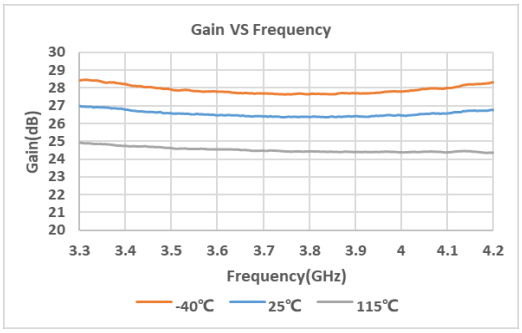

Fig. 5. Gain vs. Frequency

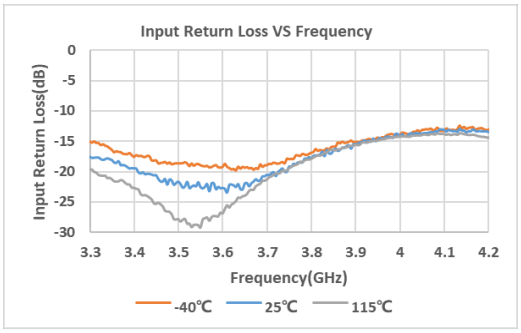

Fig. 6. Input Return Loss vs. Frequency

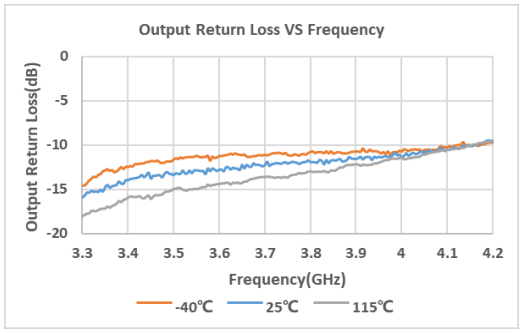

Fig. 7. Output Return Loss vs. Frequency

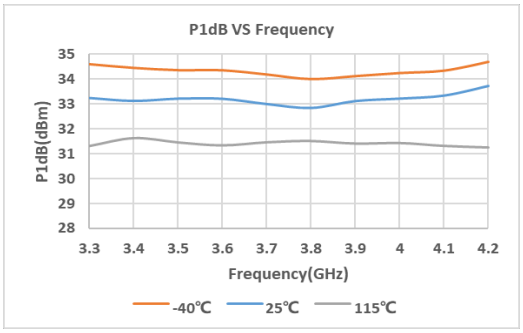

Fig. 8. P_{1dB} vs. Frequency

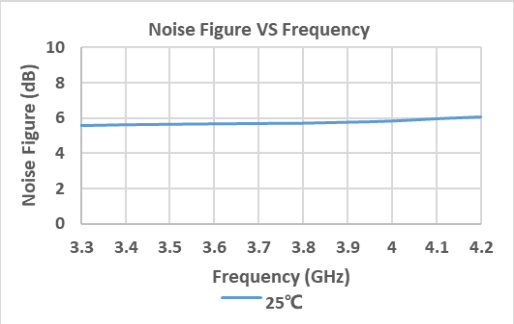

Fig. 9. Noise Figure vs. Frequency

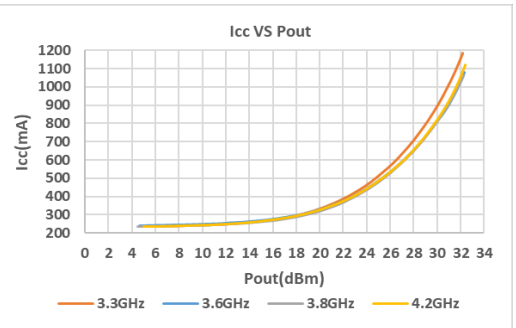

Fig. 10. I_{cc} vs. P_{out}

Package Dimensions

Typical Part Marking is shown in Figure 11 (may be different). Package Dimensions are shown in Figure 12. The PCB layout footprint for SI8B3312Q is shown in Figure 13.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SI8B3312Q is rated to Moisture Sensitivity Level 3 (MSL3) at 260°C. It can be used for lead or lead-free soldering. Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

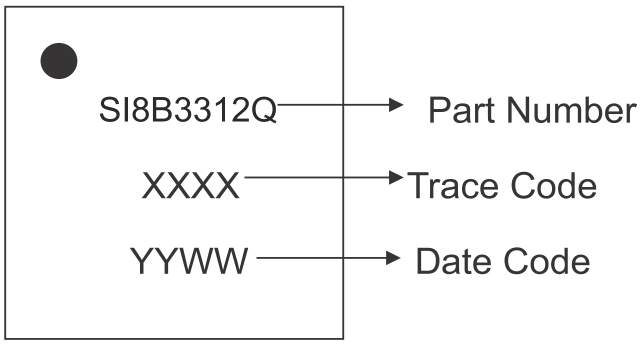

Fig. 11. SI8B3312Q Typical Part Marking
(Marking may be different)

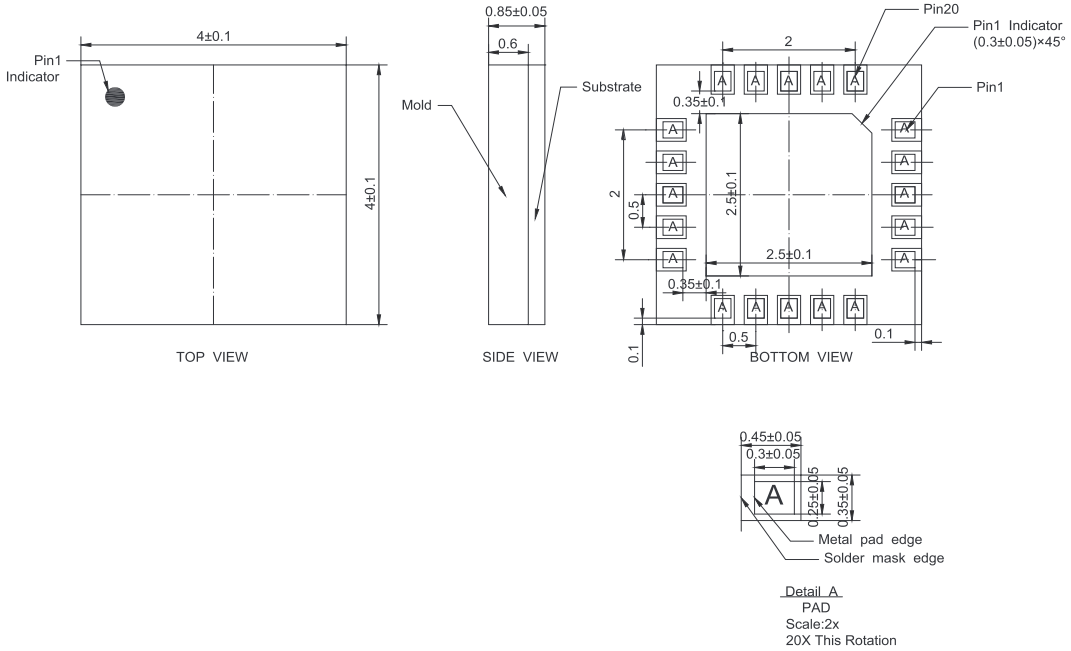

Fig. 12. SI8B3312Q Package Dimensions

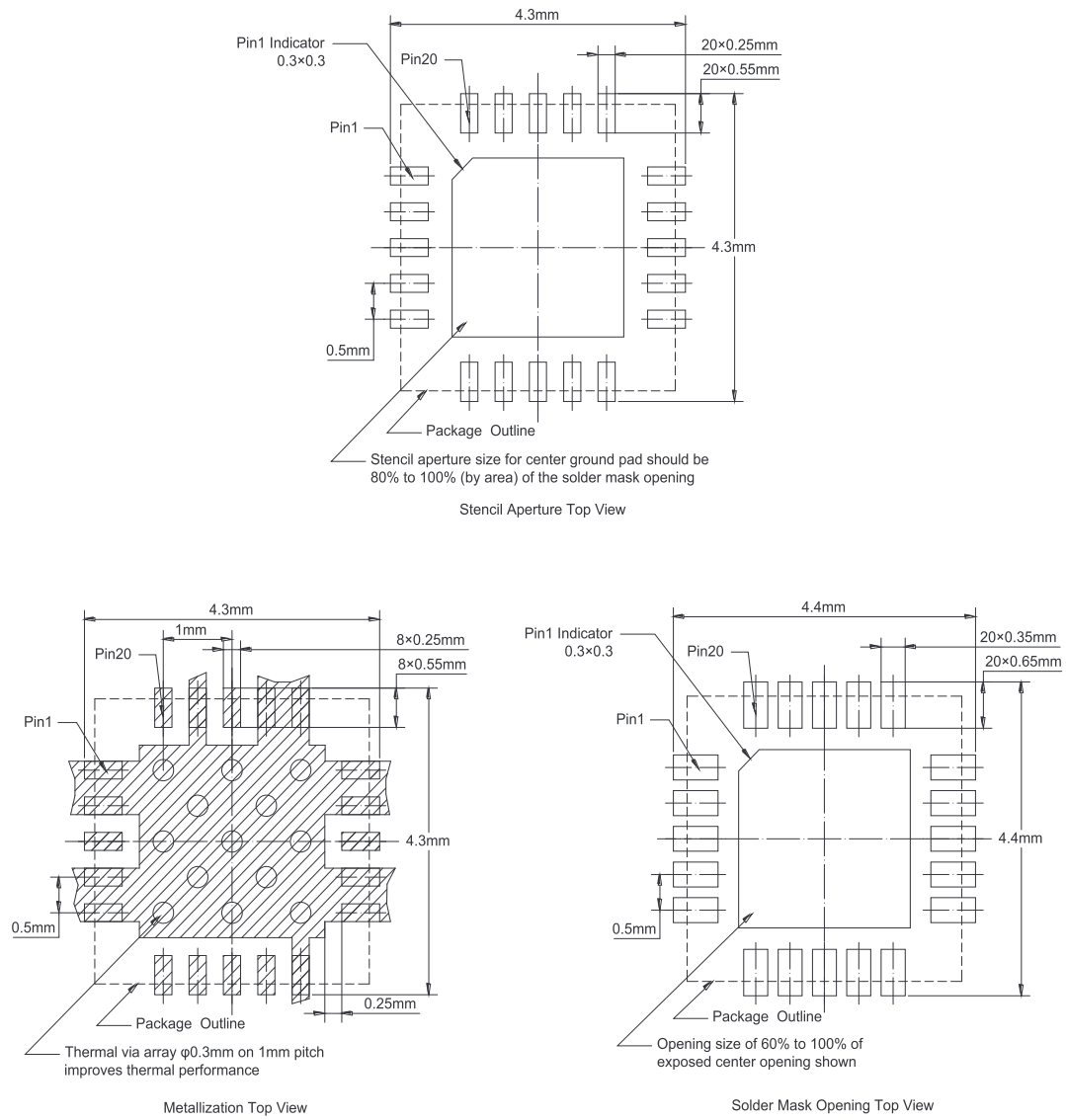

Fig. 13. SI8B3312Q PCB Layout Footprint